What is Claimed Is:

1. A modulator for receiving sample values and generating digital signals using selectable programs for implementing respective delta sigma algorithms.

2. The modulator of claim 1 in which at least one program can generate a delta sigma algorithm of selectable order N.

3. The modulator of claim 1 in which said sample values are stored into a first in first out memory element.

4. An integrated circuit containing a delta sigma modulator that can be programmed for different delta sigma algorithms.

5. An integrated circuit containing a delta sigma modulator that can be programmed for different delta sigma rates.

6. A method of designing an integrated circuit, comprising the step of providing a programmable delta sigma modulator.

7. The method of claim 6 in which said step of providing a programmable delta sigma modulator further comprises the step of providing an input port on said integrated circuit to be used to receive different programs for said programmable delta sigma modulator.

8. A method of fabricating an integrated circuit, comprising the step of providing a programmable delta sigma modulator.

9. The method of claim 8 in which said step of providing a programmable delta sigma modulator further comprises the step of providing an input port on said integrated circuit to be used to receive different programs for said programmable delta sigma modulator.

10. The modulator of claim 2, in which an algorithm of order N can be implemented by selecting a coefficient set from among plural coefficient sets.

11. The integrated circuit of claim 4 in which different algorithms are implemented using by changing a particular architecture of the circuitry used to perform operations in response to at least one control signal.

12. The integrated circuit of claim 11 in which a particular architecture is a one using multipliers.

13. The integrated circuit of claim 11 in which a particular architecture is a one using no multipliers but only shifts and adds.

14. The integrated circuit of claim 11 in which a particular architecture is a one using a pipelined architecture.

15. The integrated circuit of claim 11 in which a particular architecture is a one using a hybrid memory system.

16. The integrated circuit of claim 11 in which a particular architecture is a one using a register file arrangement.

17. The integrated circuit of claim 4 in which said at least one control signal is provided by a sequencer.

18. The integrated circuit of claim 4 in which said delta-sigma modulator has an output with controllable delays.

19. The integrated circuit of claim 4 having two delta sigma modulators, each having an independently controllable output delay.

20. The integrated circuit of claim 19 in which the independently controllable delay is a serial shift register with a selectable number of active stages.

21. A method of aligning test signals for two diverse devices connected to an integrated circuit having two respective test modulators, comprising the step of controlling the respective output delay of the two test modulators so that signals received from each of said two diverse devices are substantially phase aligned.